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Steep-switching electronic devices and a bio-inspired perspective

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Highlights:

- We review steep-slope devices surpassing 60 mV/dec.
- We draw analogies from sub-60 mV/dec switching in biological channels.
- We propose a unified multi-charge-transfer model for steep switching.

Abstract: Rapid scaling of transistor dimensions has intensified power-consumption challenges in modern microelectronics. The subthreshold slope (*SS*) quantifies the gate-voltage change required for a decade change in drain current and fundamentally limits both static and dynamic power dissipation. In conventional semiconductor transistors, the *SS* is constrained by the Boltzmann limit of about 60 mV/dec at room temperature. It is of great importance to explore materials and device strategies to surmount this thermodynamic limit. In this perspective, we first briefly outline the fundamental law that governs the 60 mV/dec switching limit in traditional metal-oxide-semiconductor field effect transistors (MOSFETs). Then we critically review emerging approaches that have demonstrated potential to surpass this 60 mV/dec limit, including device architectures like tunnel FETs (TFETs), negative-capacitance FETs (NCFETs) and nano-electro-mechanical (NEM) switches. Furthermore, we discuss the operational principle of a biological switch—voltage-sensitive ion channels, which manifest evident sub-60 mV/dec switching behaviors. Inspired by such a biological phenomenon, we develop a unified, multi-charge based interpretation to explain the steep *SS* performance in these non-conventional electrical, mechanical and biological switches. This perspective would suggest potential paradigm-shift approaches to realize ultra-steep-slope and low-power electronics.

Keywords: subthreshold slope; steep-slope switching; transistors

1. Introduction

The burgeoning applications of internet of things, cloud computing, big data, artificial intelligence, and 5G technologies have dramatically increased demands on microelectronics, elevating its strategic importance in both economic and defense sectors. Field-effect transistors (FETs), as fundamental building blocks of electronic circuits, serve critical functions as switches and amplifiers in integrated

circuits. Since the invention of the integrated circuit (IC), Moore's Law [1] has governed progress in semiconductor technology. However, as feature sizes scale below 5 nm, quantum effects—such as direct tunneling, Coulomb blockade [2], and Fermi-level pinning [3]—become significant. These phenomena signify a slowdown of Moore's Law, ushering the microelectronics industry into the post-Moore era and presenting unprecedented challenges for IC development.

While device performance has improved steadily, power dissipation has emerged as the primary bottleneck. As transistor density increases, power density rises dramatically. For example, over the past three decades CMOS gate lengths have shrunk by 10^2 times, whereas energy density has surged by ~10^4 times [4]. This unsustainable trend has made power consumption a critical constraint on microelectronics advancement. Addressing this challenge has spurred development of low-power device architectures. In particular, transistors with large subthreshold conductance are of great interest because they can achieve ultralow static power and superior switching, making them pivotal for future energy-efficient electronics [5].

The subthreshold slope (*SS*) quantifies the change of gate voltage required to modulate the drain current by one decade in the transistor's switching curve [6]. A small *SS* value is beneficial in two main respects. First, a smaller *SS* reduces the off-state leakage current, thereby lowering static power consumption. In digital circuits, even off-state transistors draw a leakage current, contributing to energy loss. Steeper subthreshold slopes suppress the leakage current for a given gate voltage, which is crucial for extending battery life and improving energy efficiency. Moreover, during switching, a device with a small *SS* achieves the on/off transition with minimal gate voltage swing, reducing the dynamic energy required per transition. Second, a smaller *SS* enables faster switching speed. With a steeper *SS*, the transistor can toggle between on and off states with a smaller change in gate voltage. This rapid transition capability allows higher switching frequencies, enhancing processor clock rates and overall system performance. Fundamentally, switching of conventional transistors is limited by the thermodynamic distribution of carriers, which imposes a lower limit of ~60 mV/dec for *SS* at room temperature (also known as the Boltzmann tyranny) [7].

This paper not only introduces the principle of the classical *SS* limit and summarizes emerging device strategies to overcome it, but also proposes an alternative, bio-inspired explanation for these approaches. Section 2 describes the fundamental *SS* limit of conventional metal-oxide-semiconductor field effect transistors (MOSFETs). Section 3 summarizes existing approaches to reduce *SS*, with representative examples including ferroelectric gate transistors nano-electro-mechanical switches. Section 4 presents conductance characteristics of voltage-gated ion channels in biological cells, and illustrates their steep-switching mechanisms. Finally, Section 5 proposes a multi-charge based theorem to analytically interpret the above concepts and Section 6 concludes the paper.

2. Subthreshold characteristics of conventional transistors

Figure 1a illustrates a typical MOSFET structure made of a silicon (Si) NMOS device. It employs a p-type Si substrate, with heavily n-doped source and drain regions. Applying a gate-to-source voltage (V_{GS}) above the threshold (V_T) induces a conductive n-type channel between the source and drain, enabling the drain-to-source current (I_{DS}) flow and transistor switching functionality. Figure 1b plots its transfer characteristic curve (I_{DS} *vs.* V_{GS}). Ideally, when V_{GS} is below V_T, the transistor should be completely off, with I_{DS} rapidly dropping to zero. In reality, however, when V_{GS} lies tens to hundreds of millivolts (mV) below V_T, the device enters the weak-inversion (subthreshold) regime. In this regime, a weakly conductive

channel still forms, and the drain current decays exponentially with V_{GS}. This exponential behavior defines the subthreshold region, where current arises from carriers thermionically surmounting the channel potential barrier. As illustrated in Figure 1c, increasing V_{GS} slightly raises the number of electrons that can overcome the barrier, thereby increasing the subthreshold drain current. For most non-degenerated semiconductors, the carrier distribution can be approximated with Maxwell–Boltzmann statistics, by which the subthreshold current is related to the carrier concentration n within the channel:

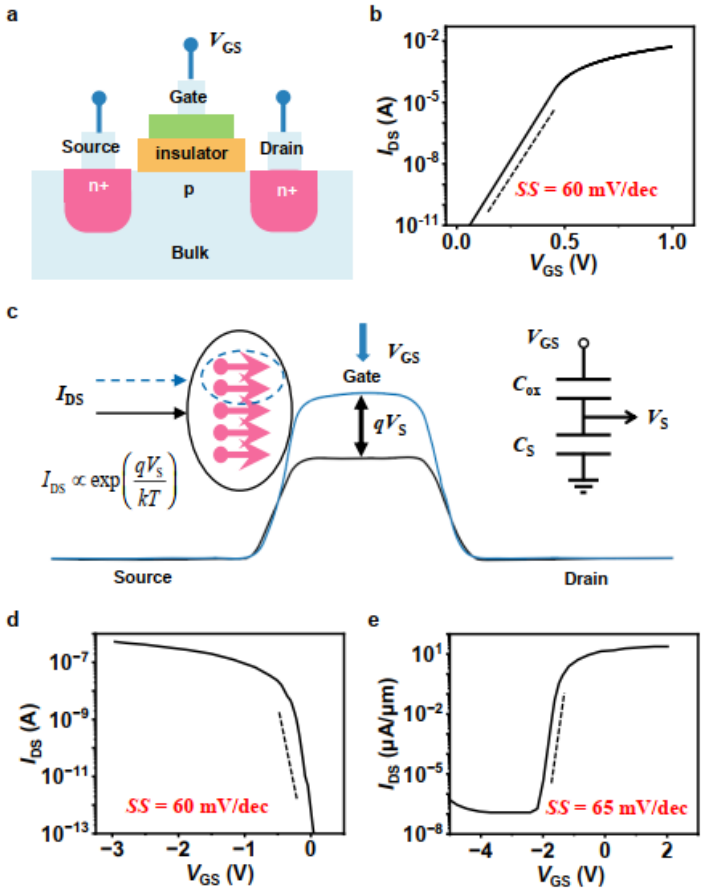

Figure 1. Subthreshold behaviors of conventional field effect transistors (FETs). **(a)** Schematic structure; **(b)** Transfer characteristic curve (I_{DS} vs. V_{GS}) of a typical silicon-based MOSFET; **(c)** Schematic interpretation of the subthreshold behavior using the electronic band. **(d)** Transfer characteristic curve of a transistor based on organic semiconductors [8]. Reprinted with permission. Copyright 2019, American Association for the Advancement of Science; **(e)** Transfer characteristic curve of a transistor based on 2D materials [9]. Reprinted with permission. Copyright 2014, John Wiley & Sons.

$$I_{DS} \propto n \propto \exp\left(\frac{qV_S}{kT}\right) \quad (1)$$

Here we assume the leakage current is minimal and negligible. q is the unit charge (1.6×10^{-19} C), k is the Boltzmann constant (1.38×10^{-23} J/K), T is the temperature, and V_S is the surface potential in the semiconductor channel. The relationship between the applied gate-to-source voltage (V_{GS}) and the surface potential (V_S) is governed by capacitive voltage division, as illustrated in Figure 1c. Specifically, V_S represents the fraction of V_{GS} that effectively drops across the semiconductor channel, and is given by:

$$V_S = V_{GS}\frac{C_{ox}}{C_{ox}+C_S} \tag{2}$$

where C_{ox} and C_S are the capacitances of the gate oxide and the semiconductor channel, respectively. Therefore, the subthreshold slope (*SS*) can be derived as:

$$SS = \frac{dV_{GS}}{d\log I_{DS}} = \frac{dV_S}{d\log I_{DS}}\cdot\frac{dV_{GS}}{dV_S} = \frac{kT\ln 10}{q}\cdot\left(1+\frac{C_S}{C_{ox}}\right) \geq \frac{kT\ln 10}{q} \tag{3}$$

At room temperature (T = 300 K), *SS* for classical transistors has a minimum value of about 60 mV/dec, which is also known as the thermionic or the Boltzmann limit. In practice, the existence of parasitic capacitances (C_S/C_{ox}) increases *SS*. This value serves as an indicator of the leakage current increase and energy loss during switching. Besides Si FETs, researchers have reported devices based on various semiconductors approaching the same thermionic limit (*SS* ≈ 60 mV/dec). For instance, Figure 1d showcases the transfer characteristics of an organic semiconductor FET based on C8-BTBT [8] (*SS* = 60 mV/dec), while Figure 1e presents data from transistors utilizing a two-dimensional semiconductor (MoS_2) [9] (*SS* = 65 mV/dec). These representative transistors with different material compositions and device structures demonstrate that the *SS* limit is a fundamental thermodynamic constraint.

3. Strategies to realize a steep subthreshold slope

In the past decades, there have been significant efforts in the microelectronics community to break the Boltzmann limit, and researchers have achieved remarkable progress in demonstrating transistors with a steep *SS* (< 60 mV/dec). Here we provide a brief summary of previously reported strategies for devices with a steep *SS*, and introduce the current theories to understand their performance.

To overcome the thermodynamic limit, one strategy is to modify the carrier transport mechanism and leverage the quantum effect of electrons by redesigning the device architecture. Examples include tunnel field-effect transistors (TFETs) [10,11] and impact-ionization MOSFETs (I-MOS) [12,13], which exploit band-to-band tunneling or impact ionization to achieve a steeper *SS*. Alternatively, approaches without harnessing quantum effects are also feasible. These concepts involve replacing the conventional single-well dielectric with materials that have metastable double-well energy landscapes. Representative implementations of this approach are ferroelectric FETs (FeFETs) [14,15], nano-electro-mechanical FETs (NEMFETs) [16,17] and nano-electro-mechanical relays (NEM relays) [18,19].

FeFETs incorporate a ferroelectric material as the gate dielectric [20]. As shown in Figure 2a, the ferroelectric layer replaces the standard oxide layer in a MOSFET. Ferroelectrics exhibit an S-shaped polarization–electric field (*P*–*E*) hysteresis (Figure 2b) due to intrinsic dipole switching under applied fields [14]. When mapped to an electrical circuit, this behavior yields an S-shaped charge–voltage (*Q*–*V*) characteristic with a negative differential capacitance region ($dQ/dV < 0$). In operation, the ferroelectric's polarization state modulates the transistor's threshold voltage: the OFF state corresponds to one polarization (high V_T) and switching to the opposite polarization rapidly lowers V_T. The negative-capacitance effect during polarization reversal effectively provides internal voltage amplification, which steepens the device's transfer switching slope [21]. Recent experiments have demonstrated FeFETs achieving sub-60 mV/dec *SS* [22–25], validating this approach. The physical mechanism and its successful implementation are illustrated in Figure 2c and Figure 2d, respectively. The theoretical model in Figure 2c predicts that the negative capacitance effect provided by the ferroelectric

gate can amplify the internal voltage, leading to a steeper transfer characteristic with a pronounced hysteresis loop [25]. This prediction is validated by the experimental results in Figure 2d, where a measured FeFET exhibits a sharply switching transfer curve with a minimum *SS* well below the 60 mV/dec limit [22]. The agreement between the theory and the measured switching confirms the ferroelectric gate's role in effectively modifying the surface potential to enable steep-slope operation. However, the inherent polarization hysteresis in ferroelectric materials remains a critical challenge, as it can cause variability and reliability issues in circuits [26]. Current research thus focuses on engineering ferroelectric materials and device structures to mitigate hysteresis while preserving the beneficial steep-slope operation.

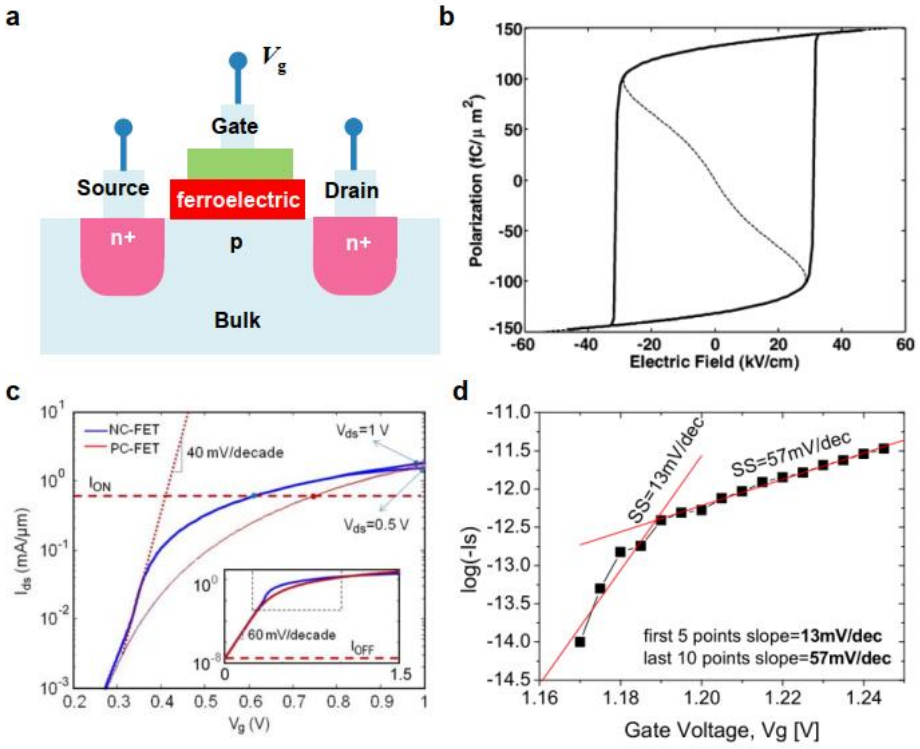

Figure 2. Ferroelectric gate field effect transistors (FeFETs). **(a)** Schematic structure of a typical FeFET; **(b)** Polarization (*P*) *vs.* electric field (*E*) for a typical ferroelectric material calculated based on the Landau–Khalatnikov equation with parameters obtained from barium titanate ($BaTiO_3$). The dashed line shows the negative d*P*/d*E* region [14]. Reprinted with permission. Copyright 2008, American Chemical Society; **(c)** Theroretically modeled transfer characteristic curves for steep-switching FeFETs [25]. Reprinted with permission. Copyright 2010, Institute of Electrical and Electronics Engineers; **(d)** Measured transfer characteristic curves for steep-switching FeFETs with ferroelectric gates, showing *SS* < 60 mV/dec [22]. Reprinted with permission. Copyright 2008, Institute of Electrical and Electronics Engineers.

Another mechanism to realize steep switching behaviors relies on electrically triggered mechanical swings. A nanoelectromechanical FET (NEMFET) is an electromechanical switch where the gate electrode is suspended over a cavity rather than separated by a solid oxide. The gate acts like a flexible spring membrane, and gate voltage is used both to induce inversion charge and to electrostatically pull the gate membrane [16,17,27]. In the OFF state, the gate is pulled upward, increasing the channel separation (oxide gap) and depleting the channel. As the gate voltage increases, the electrostatic force

pulls the gate downwards, closing the gap and enabling channel formation (Figure 3a). This mechanical action effectively amplifies the surface potential. The typical transfer characteristics of a NEMFET can exhibit multiple steep-slope regimes, reflecting the dynamic evolution of its internal charge state. As shown in Figure 3b, the three distinct subthreshold slopes, labeled curves (1), (2), and (3), correspond to successive measurement cycles. They originate from the redistribution of pre-existing positive charges in the gate oxide and at the interface, a phenomenon specific to devices fabricated with a polyimide sacrificial layer, which eventually stabilizes after several cycles [27].

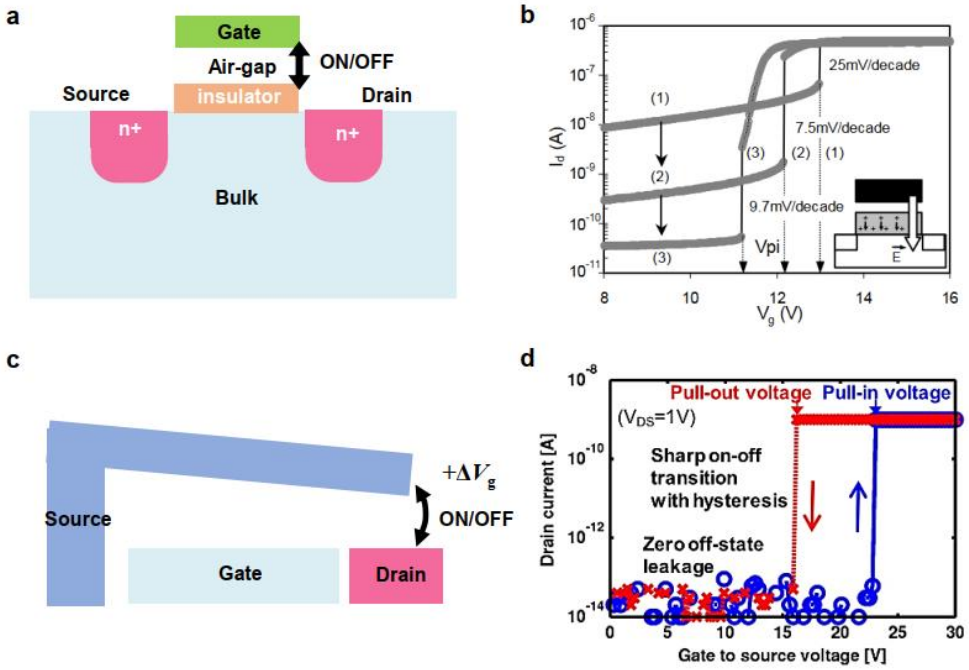

Figure 3. Nano-electro-mechanical field effect transistors (NEMFETs) and nano-electromechanical relays (NEM relays). **(a)** Schematic structure and operation principle of a typical NEMFET; **(b)** Measured transfer characteristics of a typical NEMFET showing three distinct operating regimes (labeled 1, 2, and 3) observed during successive measurement cycles. These regimes result from the dynamic redistribution of pre-existing positive charges in the gate oxide and at the interface, with the characteristic stabilizing after several cycles [27]. Reprinted with permission. Copyright 2005, Institute of Electrical and Electronics Engineers; **(c)** Schematic structure and operation principle of an NEM relay; **(d)** Measured transfer characteristic curves of a typical NEM relay [18]. Reprinted with permission. Copyright 2009, Association for Computing Machinery.

One challenge with basic NEMFET designs is that increasing the air gap in the OFF state can also increase leakage current (I_{OFF}). A proposed solution utilizes accumulation-mode or junctionless FETs [16]. In this design, the gate is initially pulled down in the OFF state to completely deplete the channel; turning the device ON is achieved by raising the gate rather than by pushing it down further. Simulations indicate that this scheme can reduce I_{OFF} by on the order of 10^5 for an air gap of 1 nm (with channel doping 10^{18} cm^{-3}, body thickness 10 nm, and gate length 25 nm). However, fabricating a reliably controlled 1-nm air gap remains highly challenging with current technology.

The nano-electro-mechanical (NEM) relay is a simple yet innovative mechanical switch that operates via electrostatic actuation, illustrated in Figure 3c. Its basic structure consists of a metal

cantilever beam serving as the channel, eliminating the need for inversion charge control. In such devices, the gate voltage generates an electrostatic force that physically moves the beam up or down, mechanically connecting or disconnecting the source and drain terminals. The transfer characteristics of NEM relays exhibit an abrupt switching behavior with inherent hysteresis (Figure 3d), primarily caused by contact forces and stiction effects. This unique property has enabled the development of complementary logic gates with energy recycling, where the potential energy stored in the bent cantilever beam facilitates oscillation between ON and OFF states, improving energy efficiency.

Notable progress has been accomplished in reducing the operating voltage (< 1 V) by scaling down device dimensions, such as implementing a 5 nm air gap, 10 nm-thick cantilever, and 100 nm gate length [28]. However, a major challenge remains contact reliability, particularly in preventing stiction and material damage (the so-called "Hammer effect") during high-speed switching. While NEM relays show promise for ultra-low-power logic circuits, their switching speed limitations make them more suitable for nonvolatile memory applications with energy-recycling capabilities, offering a balance between performance and reliability [19,29]. Future advancements in materials and nanofabrication techniques could further enhance their feasibility for next-generation computing systems.

4. Voltage-gated ion channels

In biological systems, voltage-gated ion channels are a class of transmembrane proteins found in numerous cells that exhibit variable ion permeabilities and conductivities. For example, excitable cell membranes contain potassium (K^+) and sodium (Na^+) channels that open or close in response to changes of the membrane potential [30]. When the membrane is stimulated, the potential alters, triggering the channels to open or close through movements of so-called gating charges, as illustrated in Figure 4a [31,32]. This gating mechanism is analogous to the operation of classical FETs, in which an applied voltage modulates a barrier to control the current flow.

In the 1950s, Hodgkin and Huxley conducted pioneering experiments on the squid giant axon using patch clamp techniques, leading to the development of the Hodgkin-Huxley model. This groundbreaking model successfully simulated action potential generation through iterative algorithms and established the relationship between membrane conductance and membrane potential. Notably, the slope in the linear region of their conductance–voltage relationship corresponds conceptually to a transistor's subthreshold slope. This observation highlights a deep analogy: the exponential dependence of ionic conductance on voltage in these ion channels is similar to the exponential I–V relationship in a FET's subthreshold regime [33].

These molecular switches that control ionic currents have been widely investigated by biologists and neuroscientists, but often neglected by the microelectronics community. In fact, these voltage-gated ion channels follow the same thermodynamic principle as those above-mentioned solid-state devices. Specifically, scientists have identified fundamental parallels between neuronal ion channels and FETs, where carrier transport is primarily driven by diffusion rather than drift. In FETs, electrons and holes carry current through n-type or p-type channels. Across cell membranes, ion charges flow in and out of cells through a large number of selective ion channels. Although ion channels and electronic channels employ different charge carriers, these two channel types share the following fundamental physical similarities: (1) Diffusion is the dominant carrier transport mechanism in the subthreshold

region; (2) Current through individual channels exhibits stochastic behavior; (3) Both types of channels have energy barriers that can be modulated by gated voltage.

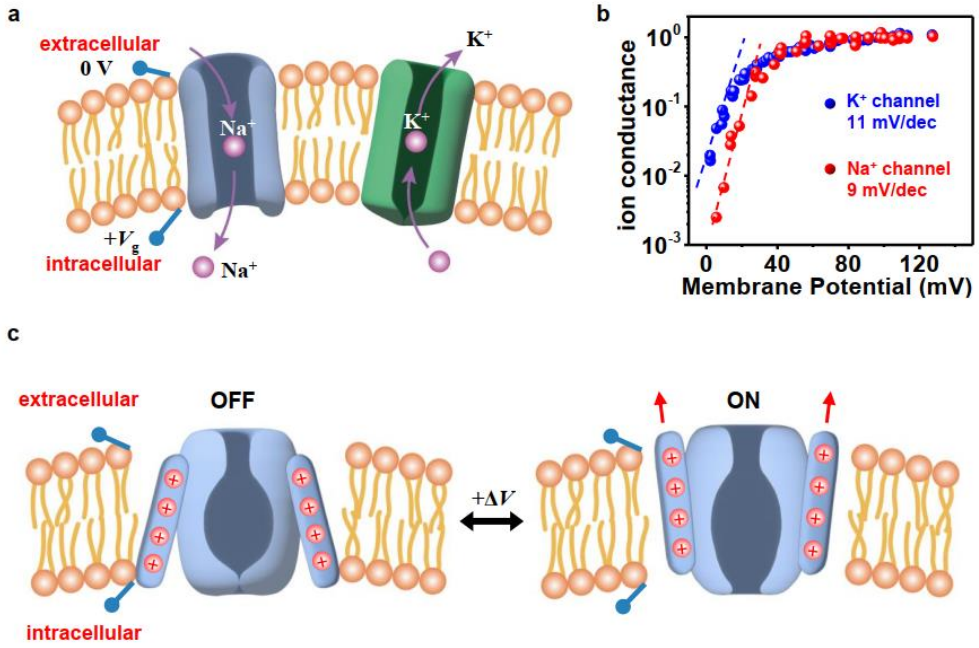

Figure 4. Voltage gated ion channels. **(a)** Schematic structure and operational principle of voltage gated ion (Na^+ and K^+) channels; **(b)** Subthreshold behaviors of Na^+ and K^+ ion channels (data extracted from the reference [34]. Reprinted with permission. Copyright 1952, John Wiley & Sons); **(c)** Schematic illustration of the open and closed states of a voltage-gated ion channel, showing the conformational changes under different membrane potentials.

In cell membranes, the energy barrier originates from the dielectric constant mismatch between the lipid bilayer and the aqueous layers. In FETs, the energy barrier arises from the bandgap difference between the semiconductor layer and the dielectric layer. Thermodynamically, the energy distributions of both ion and electrons obey Boltzmann statistics at the macroscopic level. The Boltzmann statistics governing ion and electron channel transport in the subthreshold regime establish an isomorphic physical foundation between biological ion channels and solid-state electronic channels at the atomic scale.

Similar to FETs, one can measure the conductance as a function of applied bias and analyze the subthreshold behaviors for voltage-gated ion channels. Intriguingly, experimental results reveal that these biological channels possess exceptionally steep switching. With conductance–voltage data collected in the literature [34] (Figure 4b), we find that Na^+ and K^+ channels have *SS* values of only about 9 mV/dec and 11 mV/dec, respectively. These values far surpass the Boltzmann limit (60 mV/dec) for solid-state transistors.

A plausible explanation for this strikingly steep *SS* is that each ion channel comprises peptide chains carrying multiple elementary charges. These molecular configurations have been verified by structural biologists [35,36]. The conformational transition between ON and OFF states of such a channel is schematically illustrated in Figure 4c, highlighting the voltage-driven movement of gating charges within the channel. In Equation (4), the unit charge q is replaced by a general charge $Q = Zq$:

$$SS \geq \frac{kT\ln 10}{Q} = \frac{kT\ln 10}{Zq} = \frac{60}{Z}\ \text{mV/dec} \quad (4)$$

The number of charges Z is typically 4–6. Therefore, the calculated SS values are in accordance with the experiments (10–15 mV/dec).

5. Unified theory for SS below 60 mV/dec

The interpretation of the sub-60 mV/dec swing behavior for biological ion channels inspires us to develop a unified theory for understanding the device operation with steep SS, still within the thermodynamic regime. Illustrated in Figure 5a, the voltage-gated ion channels can be considered as a nanoscale mechanical switch containing multiple (Z) charges. For each channel, its switching between ON and OFF states can be considered as an electrochemical half reaction:

$$A^{OFF} + Ze \rightleftharpoons A^{ON} \quad (5)$$

We have the Nernst equation:

$$E = E_0 - \frac{RT}{ZF}\ln\frac{[A^{ON}]}{[A^{OFF}]} \quad (6)$$

Here R is the ideal gas constant (8.314 J/mol/K), and F is the Faraday constant (96485 C/mol). E_0 is the ground-state Gibbs free energy of the system, and E is the system energy after some channels are turned on. If a gate voltage V_g is applied, $E = qV_g$. $[A^{ON}]$ and $[A^{OFF}]$ are the concentrations of channels in ON and OFF states, respectively. In the subthreshold regime, most channels are off, so $[A^{ON}] << [A^{OFF}]$ and $[A^{OFF}]$ is almost a constant. If we neglect the leakage current, the system's conductance, as well as the current flow I_{DS}, is directly proportional to the concentration of channels at the ON state $[A^{ON}]$:

$$I_{DS} \propto [A^{ON}] = [A^{OFF}]\cdot\exp\left[\frac{ZF}{RT}(qV_g - E_0)\right] \propto \exp\left(\frac{ZFq}{RT}V_g\right) \quad (7)$$

At T = 300 K, SS can be derived as:

$$SS = \frac{dV_g}{d\log I_{DS}} = \frac{RT\ln 10}{ZFq} = \frac{60}{Z}\ \text{mV/dec} \quad (8)$$

It is not surprising that this conclusion agrees with Equation 4, since the Nernst equation (Equation 6) is originated from the Boltzmann distribution. The fact that multiple charges are involved in each switching event underlies the ultra-low subthreshold slope in ion channels. When these charges move cooperatively during channel opening, they cause a much larger conductance boost per unit voltage than a single-charge process.

The above analysis can also be applied to interpret the steep swing process for those NEM devices described in Figure 3, which previously have only been vaguely explained in the thermodynamic aspect. From the perspective of our unified model, the collective mechanical motion in these switches may be conceptually analogous to a channel governed by a large number of charges (Z >> 1), which would lead to an SS approaching zero. Furthermore, FeFETs in Figure 2 probably comply with the similar mechanism, in which the ferroelectric materials contain domains of polarizable charges forming dipoles under applied bias. Figure 5b describes a hypothetical model to understand the FET with steep SS, in which a multi-charge process is involved to electrically modulate the conduction states of the elements

in the channel. This assertion of course would require further experimental evidence and theoretical analysis to support it. Nevertheless, such a cooperative charge transfer mechanism suggests a novel design paradigm: if a solid-state device could involve multiple charges per switching event, it could achieve a sub-60 mV/dec swing.

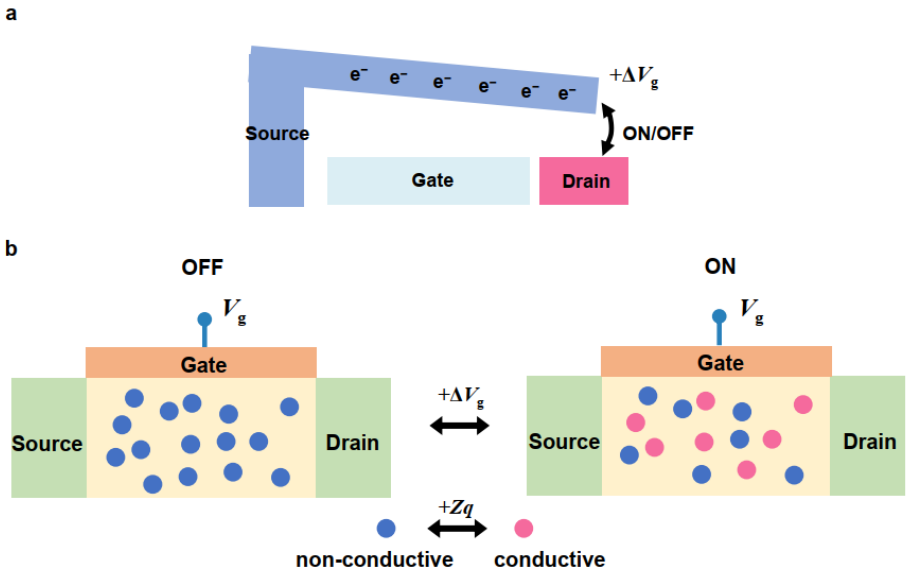

Figure 5. A bio-inspired, unified theory to interpret the steep *SS* behavior: a multi-charge effect caused by voltage gating. **(a)** Schematic of a mechanical multi-electron transfer switch model illustrating the gating mechanism through conformational change; **(b)** A field-effect transistor-like switch, where a multi-charge process is involved to modulate the conduction states of the elements in the channel.

6. Conclusion

In this perspective, we have surveyed the fundamental *SS* constraint of conventional MOSFETs and reviewed emerging architectures, including TFETs, I-MOS, FeFETs and NEMFETs, which employ tunneling, impact ionization, ferroelectric switching, or electromechanical action to achieve steep-slope switching. Furthermore, we introduce and analyze the behaviors of voltage-gated ion channels, which are often overlooked by the microelectronics community. The exceptionally low *SS* values (~10 mV/dec) observed in these ion channels underscore the potential of correlated charge dynamics. The cooperative charge-transport paradigm presented here offers an innovative strategy to overcome the Boltzmann limit in solid-state transistors. By emulating the concerted gating of biological ion channels, where multiple charges operate synchronously to produce an ultra-steep conductance response, devices can achieve internal voltage amplification. In this framework, each additional gating charge effectively reduces the thermal *SS* floor by its valence, providing a tunable design parameter for sub-60 mV/dec operation at ambient conditions. Moreover, biological ion channels can operate through sophisticated non-equilibrium mechanisms that enable directionally biased switching. For example, a study on chloride channels revealed that the transition rates between open and closed conformations are not equal but are instead driven by the transmembrane ion concentration gradient [37]. This feature can also be emulated to design functional devices.

Translating these biological principles into semiconductor platforms entails identifying materials and device geometries that support multi-charge gating while maintaining reliability and manufacturability. Future efforts should prioritize the integration of high-valence ionic species or engineered dipolar domains within transistor gate stacks, as well as the exploration of hybrid electronic-ionic conduction in electrochemical transistor formats. Comprehensive analysis and modelling of coupled charge–voltage–mechanical interactions will be essential to optimize device performance. Ultimately, realizing bio-inspired, cooperative-charge transistors promises to enable ultra-low-power logic and memory circuits, charting a path toward next-generation energy-efficient computing architectures.

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Authors' contributions

Conceptualization, X.S.; methodology, M.L.; literature investigation and data curation, M.L.; writing—original draft preparation, M.L., Y.X. and X.S.; writing—review and editing, M.L., Y.X. and X.S.; visualization, M.L. and Y.X.; supervision, X.S.; project administration, X.S.; funding acquisition, X.S. All authors have read and agreed to the published version of the manuscript.

Conflicts of interests

The authors declare no conflict of interest.

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